

## Single phase 21 level hybrid multilevel inverter with reduced power components employing low frequency modulation technique

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### ABSTRACT

This paper introduces a new hybrid topology of multilevel inverter capable of generating 21-level output voltage. The proposed topology is built using the combination of cross-switched bridge and a conventional full H-bridge. Compared to the conventional topologies and other hybrid topologies, the newly introduced multilevel inverter has the ability to maximize the number of voltage levels utilizing lower number of DC voltage sources, integrated bipolar transistor (IGBT) switches and gate drivers. A low frequency modulation technique is used to generate the ideal multilevel output voltage and gate pulses. Furthermore, the proposed topology is validated by building a hardware prototype and obtaining relevant experimental results. The acquired simulated and experimental results indicate the proper functioning of the proposed hybrid topology along with the compatibility of the applied modulation technique.

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## 1. INTRODUCTION

Multilevel inverters (MLI) have emerged as a prospective concept in the field of high power and medium voltage regulation. As a popular power electronic device multilevel inverter has advantages and disadvantages. The most common drawback of conventional multilevel inverters is the increased usage of power components while generating high level output voltage. This specific drawback can lead to computational complexities, lower efficiencies, presence of harmonics and most importantly hinder the overall performance of an inverter [1, 2]. The idea of multilevel inverter was first proposed in 1975 [3].

Since then various MLI topologies were proposed with different abilities and functionalities. Each of these topologies was designed to improve its ability of producing increased level output voltage using low amount of power equipments, compared to its previous versions. Neutral point clamped (NPC), flying capacitor (FC) and the cascaded Hbridge (CHB); these are the three fundamental multilevel inverter topologies. The first NPC inverter was a 3 level inverter consisted of four switching devices, two cascaded capacitors and one DC supply [4]. The voltage balancing of the DC link capacitors in NPC inverter, is a decisive task since the voltage at the neutral point is always deviating. The FC MLIs use capacitors of clamping diodes.

These clamping diodes can clamp the device voltage to one capacitor voltage level. The DC-link capacitors of these inverters are arranged in a ladder structure, where the voltage differs across each capacitor from the next capacitor. Since its invention, CHB inverters have drawn great interest over other topologies because of their simplicity and modularity of control. These inverters possess some of the exceptional features including ability of generating high output voltage with reduced total harmonic distortions (THD). Furthermore, it can generate common mode voltage (CM) which reduces stress on the motor.

Although these MLI topologies have better voltage capacity and efficiency, they require increased number of power electric components to produce high output voltage. This can lead to high switching losses and increase the overall cost of the system. As a result, considerable amounts of researches were conducted. Recently, different variations of these basic MLI topologies have been developed to improve their functionalities in a cost-effective way. Some of these topologies include the active NPC (ANPC) converter. In ANPC inverters, clamping diodes were used instead of power switches to overcome the loss balancing issue between the outer and inner switches [5-7].

Due to the use of power switches, the current at the neutral point can be forced to flow in both upper and lower path of the inverter. This results in distribution of equal losses among all the semiconductor devices. A new variation of FC inverter was proposed in [8] which used a combination of serial and parallel connected flying capacitors. This version of FC inverter has better voltage capacity and high-quality output compared to its traditional counterpart. Traditional CHB inverters requires isolated DC sources of equal magnitude and multiple transformers for each cell in order to provide electrical isolation [9,10]. A variation of traditional CHB inverters known as asymmetrical CHB use DC voltage sources of different ratings. Since the DC supplies follow a certain voltage ratio, it can increase the voltage levels of the inverter significantly. In 2011, a new MLI was introduced known as multistring multilevel inverter which utilises the fundamentals of CHB inverters [11].

The basic structure of this topology is based on specific cross connecting low voltage switches and DC voltage sources. Although many MLI topologies have been developed, the optimization of the power equipment required for these inverters were given a new height via the development of the first hybrid inverter [12]. This newly found concept of hybrid topology along with the multistring MLI was the primary motivation behind designing the proposed hybrid topology. Different modulation strategies were also developed with the new multilevel inverter topologies in order to control these inverters. Generally, all the modulation techniques can be classified into two categories: low and high switching frequencies [13]. Based on this classification, this paper uses a modified low switching frequency modulation technique to generate the desired switching pulses. The operating principles of the proposed inverter are verified by both computer simulation, using MATLAB and the hardware prototype.

## 2. PROPOSED TOPOLOGY AND OPERATING PRINCIPLE

The proposed hybrid inverter was designed using the cascaded combination of a single-phase cross-switched bridge and a single cell conventional full H-bridge. The cross-switched bridge is implemented following the fundamentals of the proposed inverter in [14]. The cross bridge contains 2 back to back DC supplies (VC1 and VC2) and a total of six power switches (S1, S2, S3, S4, S5 and S6) as shown in Figure.1. The middle two switches (S5 and S6) of the cross bridge are cross connected and act as a medium between the two DC sources (VC1 and VC2). The cross bridge can be built either by using two DC supplies having same or different voltage ratings. When the cross bridge follows symmetrical configuration, it is capable of generating 5-level voltage output. On the contrary, if this bridge is built utilizing asymmetrical configuration, it is capable of generating 7-level voltage output. The hybridization is done using the asymmetrical configuration. The switching sequence of the 7-level output voltage is shown in Table 1.

Table 1. Voltage levels and switching sequences of a single-phase 7-level asymmetrical cross-switched bridge.

Switching States ( <i>a</i> )	ON/OFF Switches			Output Voltage ( $V_{ab}$ )
	<i>S1</i>	<i>S5</i>	<i>S3</i>	
6	1	0	0	$3E$
5	1	0	1	$2E$
4	0	0	0	$E$
3	1	1	0	0
	0	0	1	
2	1	1	1	$-E$
1	0	1	0	$-2E$
0	0	1	1	$-3E$

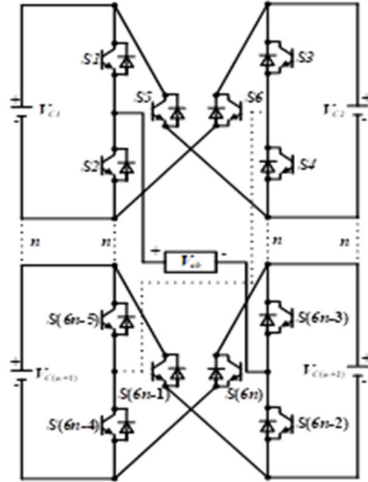


Figure 1. Single-phase NLevel cross-switched multilevel inverter

The cross-switched inverter can be extended into  $N_{Level}$  by following (1), (2) and (3) respectively.

$$N_{Level} = (6n + 1) \quad (1)$$

$$N_{Switch} = N_{Level} - 1 \quad (2)$$

$$N_{DC\_supplies} = \frac{N_{Switch}}{3} \quad (3)$$

Here,  $n = 1, 2, 3, \dots$  and it represents the number of cell of the cross-switched bridge. The bottom bridge is a traditional 3-level full H-bridge which consists of only one DC supply designated as  $V_{C3}$  and four semiconductor switches ( $S7, S8, S9$  and  $S10$ ).

The final design of the hybrid multilevel inverter has a total of ten semiconductor switches and three DC voltage sources as illustrated in Figure.2. The whole topology of the hybrid inverter can follow either symmetric or asymmetric configuration. For the symmetric configuration the hybrid topology is capable of generating 7-level voltage output. However, for the next sections of this paper, asymmetric configuration of the hybrid topology was followed and utilized. This configuration is implemented by maintaining a voltage ratio of 2:1:7 among the three DC supplies. While following this voltage ratio, the MLI has the ability to generate 21 voltage levels using a total of 21 switching sequences. The switching sequences are presented in Table 2 whereas, the switching operation of the hybrid inverter for the positive half cycle is shown in Figure.3. It can be noticed from Table 2, that the proposed inverter possesses switching redundancies for certain voltage levels. This feature increases the reliability of the inverter in case of malfunction of any switches or drivers.

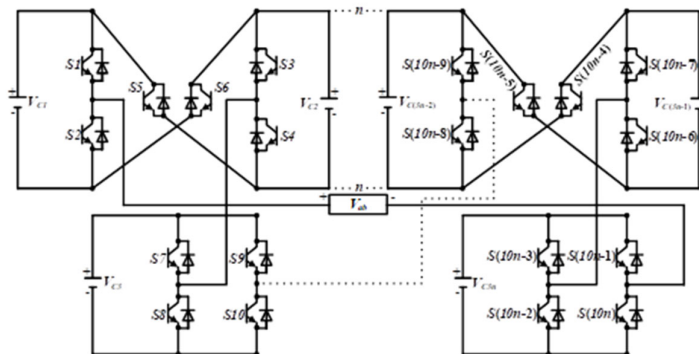


Figure 2. Single-phase NLevel hybrid multilevel inverter.

Table 2. Voltage levels and switching sequences of a single-phase 21-level asymmetrical hybrid inverter.

Switching States ( <i>a</i> )	ON/OFF Switches for upper bridge ( <i>C</i> )		ON/OFF Switches for lower bridge ( <i>H</i> )		Output Voltage ( <i>V<sub>ab</sub></i> )	
	<i>S1</i>	<i>S5</i>	<i>S3</i>	<i>S7</i>	<i>S9</i>	
20	1	0	0	1	0	10 <i>E</i>
19	1	0	1	1	0	9 <i>E</i>
18	0	0	0	1	0	8 <i>E</i>
17	1	1	0	1	0	7 <i>E</i>
16	1	1	1	1	0	6 <i>E</i>
15	0	1	0	1	0	5 <i>E</i>
14	0	1	1	1	0	4 <i>E</i>
13	1	0	0	0	0	3 <i>E</i>
	1	0	0	1	1	
12	1	0	1	0	0	2 <i>E</i>
	1	0	1	1	1	
11	0	0	0	0	0	<i>E</i>
	0	0	0	1	1	
	0	0	1	0	0	
	0	0	1	1	1	
10	1	1	0	1	1	0
	1	1	0	0	0	
	1	1	1	0	0	
9	1	1	1	1	1	- <i>E</i>
	0	1	0	0	0	
8	0	1	0	1	1	-2 <i>E</i>
	0	1	1	0	0	
7	0	1	1	1	1	-3 <i>E</i>
	0	1	1	0	0	
6	1	0	0	0	1	-4 <i>E</i>
5	1	0	1	0	1	-5 <i>E</i>
4	0	0	0	0	1	-6 <i>E</i>
3	0	0	1	0	1	-7 <i>E</i>
2	1	1	1	0	1	-8 <i>E</i>
1	0	1	0	0	1	-9 <i>E</i>
0	0	1	1	0	1	-10 <i>E</i>

Similar to the cross-switched inverter the hybrid MLI can also be extended into  $N_{Level}$  following (4), (5) and (6) respectively. It should be noted that to apply this extension the DC voltage sources should always follow 2:1:7 voltage ratio.

$$N_{Level} = (20n + 1) \quad (4)$$

$$N_{Switch} = \frac{N_{Level}-1}{2} \quad (5)$$

$$N_{DC\_supplies} = \frac{3 \times N_{Switch}}{10} \quad (6)$$

It can be observed from the switching operation in Figure.3 that the current can't form short circuit loops around the 3 DC supplies because of the switching combinations. Thus, it prevents short circuit current to flow through the 21-level hybrid multilevel inverter.

The total standing voltage of the hybrid topology is calculated following Table 2. The maximum voltage stress on each switch is calculated at off state and then these numbers are added together to get the total standing voltage (TSV) of the proposed MLI. TSV calculation is demonstrated by giving the example of the voltage stress on switch *S1*. The DC supply designated as  $V_{C1}$  is applying maximum standing voltage on *S1* when it is at off state at  $V_{ab} = -2E$ . The calculation is as follows;

$$V_{S1} = 2E \text{ (At; } V_{ab} = -2E)$$

$$V_{S2} = 2E \text{ (At; } V_{ab} = 2E)$$

$$V_{S3} = E \text{ (At; } V_{ab} = E)$$

$$V_{S4} = E \text{ (At; } V_{ab} = -E)$$

$$V_{S5} = 3E \text{ (At; } V_{ab} = 10E)$$

$$V_{S6} = 3E \text{ (At; } V_{ab} = -10E)$$

$$V_{S7} = V_{S10} = 7E \text{ (At; } V_{ab} = -10E)$$

$$V_{S8} = V_{S9} = 7E \text{ (At; } V_{ab} = 10E)$$

$$TSV = 2E + 2E + E + E + 3E + 3E + 7E + 7E + 7E + 7E = 40E$$

### 3. COMPARATIVE ANALYSIS

The characteristics of the hybrid multilevel inverter is highlighted by comparing it with traditional and recently developed multilevel inverter topologies. The comparison is done in terms of power components such as IGBT switches Figure.4a, diodes Figure.4b, diodes and DC capacitors/supplies Figure.4c. Although the proposed MLI requires same number of DC supplies as ACHB, by observing Figure.4d, it can be addressed that the proposed topology required low number of

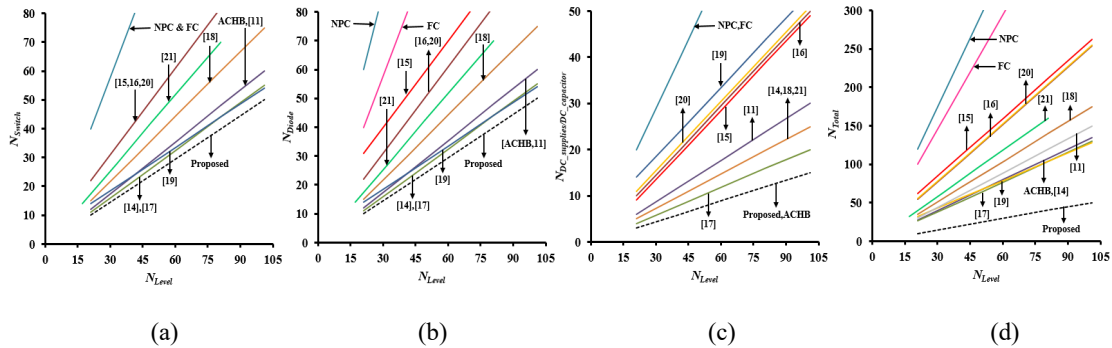


Figure 4. Comparison between different MLIs in terms of: (a) switches, (b) diodes, (c) DC supplies/capacitors and (d) total components.

Table 3. Comparison between different MLI topologies in terms of number of levels ( $N_{Level}$ )

MLI topologies	Levels* ( $N_{Level}$ )	Switches ( $N_{Switch}$ )	Diodes ( $N_{Diode}$ )	DC-links ( $N_{DC\ supplies/DC\ capacitors}$ )	TSV	Total Components ( $N_{Total}$ )
NPC		$2(N_{Level} - 1)$	$N_{Level} - 1$	$N_{Level} - 1$	$2(N_{Level} - 1)$	$4(N_{Level} - 1)$
FC		$2(N_{Level} - 1)$	$2(N_{Level} - 1)$	$N_{Level} - 1$	$2(N_{Level} - 1)$	$5(N_{Level} - 1)$
ACHB		$3(N_{Level} - 1)/5$	$3(N_{Level} - 1)/5$	$3(N_{Level} - 1)/20$	$2(N_{Level} - 1)$	$27(N_{Level} - 1)/20$
SCMLI [15]		$N_{Level} + 1$	$N_{Level} + 10$	$(N_{Level} - 3)/2$	$35(N_{Level} - 1)/4$	$(5N_{Level} + 19)/2$
SDCMLI [16]		$N_{Level} + 1$	$N_{Level} + 1$	$(N_{Level} - 1)/2$	$35(N_{Level} - 1)/4$	$(5N_{Level} + 3)/2$
CMLI [17]	$20x + 1$	$11(N_{Level} - 1)/20$	$11(N_{Level} - 1)/20$	$(N_{Level} - 1)/5$	$69(N_{Level} - 1)/20$	$13(N_{Level} - 1)/10$
AHMLI [11]		$3(N_{Level} - 1)/5$	$3(N_{Level} - 1)/5$	$3(N_{Level} - 1)/10$	$5(N_{Level} - 1)/2$	$3(N_{Level} - 1)/2$
ASTMLI [18]		$3(N_{Level} - 1)/4$	$3(N_{Level} - 1)/4$	$(N_{Level} - 1)/4$	$5(N_{Level} - 1)/2$	$7(N_{Level} - 1)/4$
SBSIMLI [19]		$(N_{Level} + 7)/2$	$(N_{Level} + 7)/2$	$(N_{Level} - 1)/5$	$9(N_{Level} - 1)/4$	$2(3N_{Level} + 17)/5$
NTPMLI [20]		$N_{Level} + 1$	$N_{Level} + 1$	$(N_{Level} + 1)/2$	$28(N_{Level} - 1)/5$	$5(N_{Level} + 1)/2$
RSMLI [14]	$18x + 1$	$(N_{Level} + 1)/2$	$(N_{Level} + 1)/2$	$(N_{Level} - 1)/4$	$99(N_{Level} - 1)/20$	$(5N_{Level} + 3)/4$
ORMLI [21]	$16x + 1$	$7(N_{Level} - 1)/10$	$7(N_{Level} - 1)/10$	$(N_{Level} - 1)/5$	$9(N_{Level} - 1)/5$	$8(N_{Level} - 1)/5$
Proposed hybrid MLI	$20x + 1$	$(N_{Level} - 1)/2$	$(N_{Level} - 1)/2$	$3(N_{Level} - 1)/20$	$2(N_{Level} - 1)$	$23(N_{Level} - 1)/20$

\* $x = 1, 2, 3, \dots$  and it signifies the augmentation of  $N_{Level}$

Power components while comparing with all the traditional MLIs. The proposed hybrid topology is again compared with nine other recently developed MLI topologies named as reduced switch multilevel inverter (RSMLI) [15], switched capacitor multilevel inverter (SCMLI) [16], switched DC multilevel inverter (SDCMLI) [17], cascaded multilevel inverter (CMLI) [18] including five hybrid topologies named as AHMLI [11], ASTMLI [19], SBSIMLI [20], NTPMLI [21] and ORMLI [22]. Detailed comparison with respect to number of levels ( $N_{Level}$ ) are demonstrated in Table 3. All of these MLI topologies follow asymmetrical configuration with a voltage ratio of 2:1:7 to justify the comparison. Observing from Table 2, for [15] voltage levels  $N_{Level} = 19, 37, 55, 73, \dots, (18x+1)$  were selected instead of  $N_{Level} = 21, 41, 61, 81, 101, \dots, (20x+1)$ . Similarly, for ORMLI [22] voltage levels  $N_{Level} = 17, 33, 49, 65, \dots, (16x+1)$  were selected. These voltage levels were chosen since, they are closest to the desired voltage levels that were used for comparison purpose in this section. Furthermore, it should be noted that the TSV of the hybrid inverter is as same  $2(N_{Level} - 1)$  as the traditional inverters. However, it still has lower TSV compare to all other MLIs except ORMLI [22]. Thus, it can be stated that the TSV of the proposed inverter is in an acceptable range. Since, ORMLI is producing voltage levels in a range of  $(16x+1)$ , it is expected that it has lower TSV compared to the proposed inverter.

#### 4. LOW FREQUENCY MODULATION

The modified modulation method applied to synthesize the gate signals of the suggested hybrid multilevel inverter topology is identified as Nearest Level Control (NLC). This control method is a low frequency technique which is implemented by choosing the appropriate voltage levels that are closest to the preferred reference output voltage [12]. The algorithm of this control technique is easily executable compare to the other control techniques. It is also highly understandable as it deals with low frequency switching states and nearest voltage level selection. In this control technique the output voltage level is decreased to a distinctive simple expression which is given by;

$$\text{Nearest voltage level} = E \times a_{\text{round}} \quad (7)$$

$E$  is demarcated as the voltage alteration between two levels which is used to normalize the desired voltage reference ( $V_{AB\_ref}$ ) and to obtain the switching conditions designated by  $a$  [22]. The resulting value is estimated by means of the round function. This function works by rounding the elements of  $a$  to the closest decimal or integer. The resulting value from this mathematical calculation will represent the closest voltage levels to the reference. Finally, the estimated values are frequently equated with corresponding values of the MLI's switching conditions stowed in a switching table which is used to determine the gate pulses. Thus, the initial reference voltage is found by using, (8) and, (9);

$$V_{AB\_ref} = \frac{mV_{dc}}{2} \sin \theta \quad (8)$$

$$V_{dc} = \sum_{i=0}^k V_{Ci} \quad (9)$$

Where,  $m$  is the modulation index which has a range of  $0 \leq m \leq 1$ ,  $\theta$  is the inverter's electrical angle,  $V_{dc}$  the total *magnitude* of DC-links supplies and  $k$  the number of DC supplies. The electrical angle can be used to introduce phase differences in case of three phase systems. In addition, a DC offset has been applied with the reference voltage so that the line to ground voltage will be in tolerable range of zero to the DC supply voltage without causing any over-modulation. After applying the DC offset the voltage has been shifted above zero and all the negative values are eliminated. The finalized reference voltage can be determined by . (10);

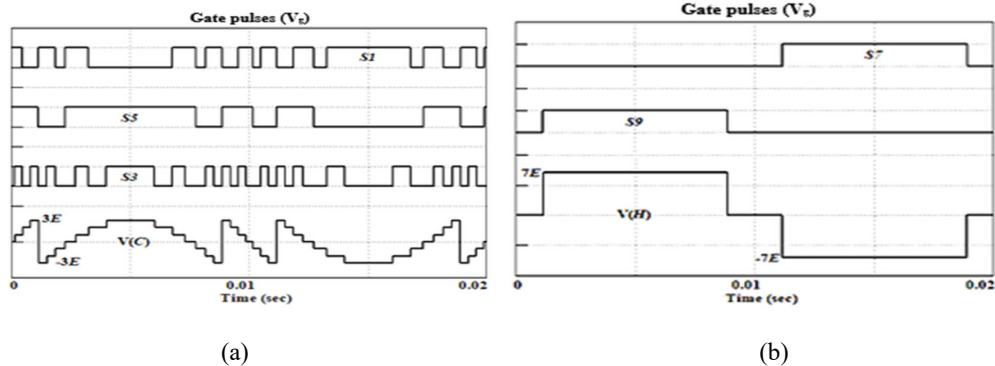
$$V_{AB\_ref(final)} = \frac{mV_{dc}}{2} \sin \theta + \frac{V_{dc}}{2} \quad (10)$$

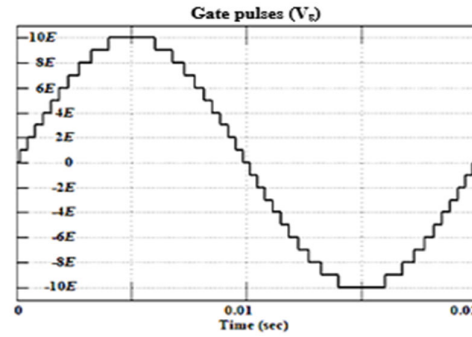
Finally, the switching states  $a$  is determined by applying the round function with respect to voltage difference  $E$  which can be defined by the . (11) and (12).

$$E = \frac{2V_{dc}}{N_{\text{Level}} - 1} \quad (11)$$

$$a_{\text{round}} = \text{round} \left( \frac{2V_{AB\_ref(final)}}{E} \right) \quad (12)$$

The obtained switching states  $a$  is further utilized by frequently comparing with a pre-generated table in order to produce the gate signals and the 21-level output of the hybrid inverter which is shown in Figure 5.





(c)

Figure. 5. Gate pulses and output voltage of: (a) cross-switched bridge, (b) H-bridge, (c) 21-level hybrid inverter.

## 5. SIMULATION RESULTS

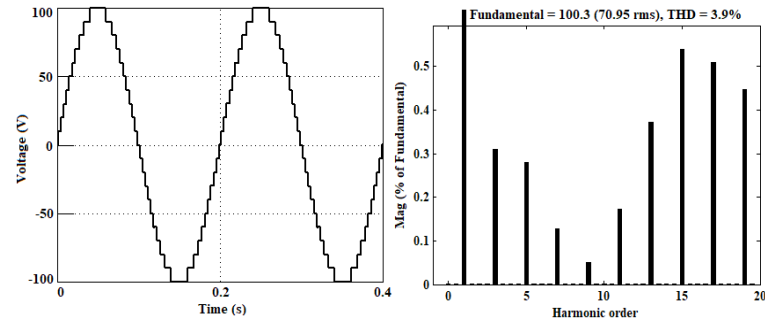
The simulation of the projected inverter was completed using MATLAB Simulink version R2014a. Simulation was done by considering a sinusoidal wave as the reference voltage waveform which has a nominal frequency,  $f = 50$  Hz. The hybrid multilevel inverter was built using three unequal DC supplies where  $V_{C1} = 20$  V,  $V_{C2} = 10$  V and  $V_{C3} = 70$  V making the whole DC voltage of the hybrid MLI to 100 V. A resistive-inductive single phase load was coupled involving  $R = 100 \Omega$  and  $L = 0.23$  H at the output side of the hybrid MLI. The output voltage of the inverter along with its THD at  $m = 1$  is depicted in Figure.6a. It can similarly be detected from Figure. 5a that the proposed MLI's output voltage has reached its maximum value  $V_{ab\_max} = 100.3$  V generating 21 voltage steps and the simulated RMS voltage is  $V_{ab\_rms} = 70.95$  V. This value is nearly close to the hypothetical value of 70.7V that can be calculated from [23, 24]:

$$V_{ab\_rms} = 0.707 \times m \times V_{peak} \quad (13)$$

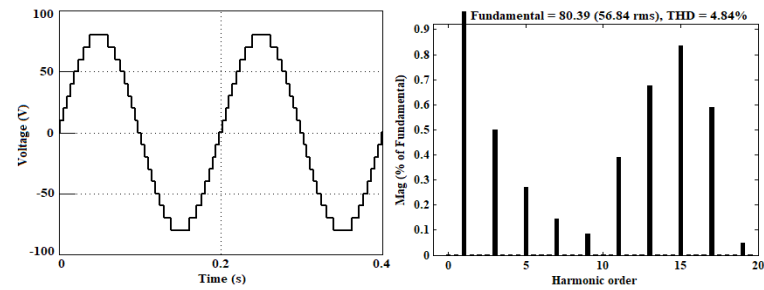
Figure.6a also approves that the THD is only 3.9% with the higher order harmonics removed completely. This also specifies the symmetric nature of the voltage waveform. In Figure.6b, the modulation index is reduced to  $m = 0.8$  and because of this both the output voltage and the RMS voltage have declined to  $V_{ab} = 80.39$  V and  $V_{ab\_rms} = 56.84$  V respectively generating 17 voltage steps. Nevertheless, the THD has amplified to 4.84% in this case since, the hybrid topology has generated lesser amount of voltage stages with respect to the earlier circumstance. Further reducing the modulation index to  $m = 0.3$  outcomes in an output voltage of  $V_{ab} = 30.62$  V with only seven voltage steps as shown in Figure.6c. Furthermore, it must be addressed from Figure.6c that the simulated RMS voltages in this case is decreased to  $V_{ab\_rms} = 21.65$  V while the THD have amplified expressively to 12.33%. The THD of the hybrid inverter with respect to other modulation indices are illustrated in Figure.7.

## 6. EXPERIMENTAL RESULTS

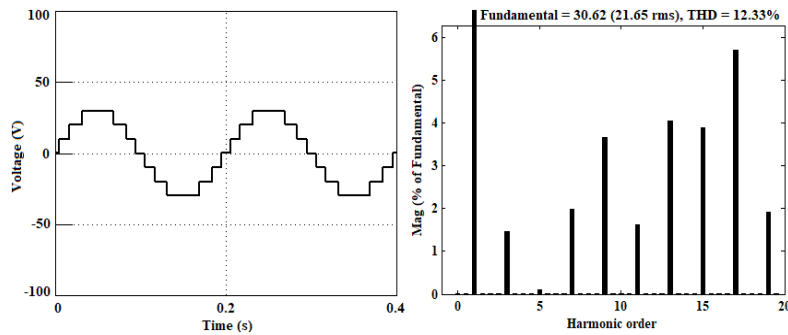
The hardware version of the hybrid MLI was established producing an integration between MATLAB Simulink and some hardware equipment. The prototype was developed applying TMS320F28335 digital signal processor (DSP) to generate the gate pulses of the MLI. The integration was established applying CCS v5 software. The gate driver signals were produced using CCS which utilized the pre-loaded gate pulses from the DSP. These gate pulses were initially loaded into DSP from MATLAB. These signals from the gate drivers are used to synthesize the experimental result.



(a)



(b)



(c)

Figure 6. Simulated results for voltage and harmonic spectrum at different modulation indices: (a) at,  $m=1$ , (b) at,  $m=0.8$  and (c) at,  $m=0.3$ .

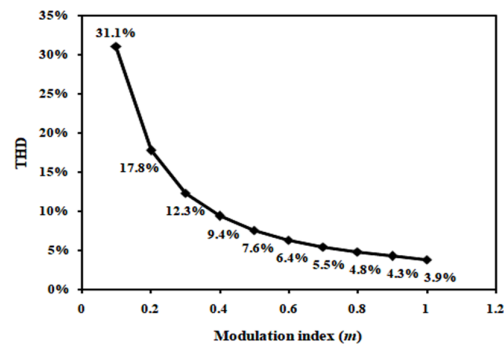


Figure 7. Simulated THD against different modulation indices



The experimental setup was done following the arrangement similar to the simulation setup. The load bank was used to connect a single-phase load to the hybrid multilevel inverter having the following parameters;  $R = 100 \Omega$  and  $L = 0.23 \text{ H}$ . The hardware parameters of the hybrid MLI are specified in Table 4. Furthermore, the control block diagram of the prototype is illustrated in Figure.8.

The performance of the hybrid MLI and the compatibility of the modulation method were additionally verified by obtaining the experimental results. The results include the analysis of harmonic spectrum under different modulation indices. Figure 9(a), Figure 10(a) and Figure 11(a) demonstrate

Table 4. Specifications of the hardware prototype

Hardware Specification	Symbol	Value/ Model
DC voltage supplies	$V_{C1}$	20 V
	$V_{C2}$	10 V
	$V_{C3}$	70 V
Fundamental frequency	$f$	50 Hz
IGBT switches	$S1-S10$	ABB 5SNG 250A and 3300 V
IGBT gate drive optocoupler		HCPL3120
IGBT gate drive IC		74HC04

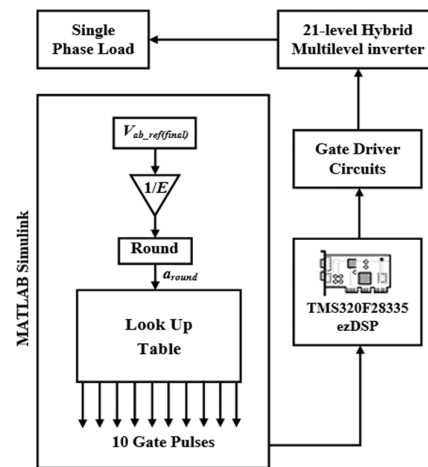


Figure 8. Control block diagram.

The proposed MLI's output voltage waveforms with respect to different modulation indices. By brief comparison, it can be confirmed that the output waveforms of the hybrid MLI both from the simulation results and the experimental results are almost identical. It can be also confirmed from the THD spectrums that all the even order harmonics are eradicated. Figure.9b has shown that the obtained THD at  $m = 1$  is only 4.5%. Additionally, it can be observed from the graph that all the triplen harmonic components (3rd, 9th and 15th) are also eliminated. The measured RMS voltage from the fundamental frequency component at  $m = 1$ , is 69.2 V. This value is almost same as the simulated value of RMS voltage 70.95 V indicating the validity of the outputs. However, in this case presence of 5th harmonic component can be observed having a normalized value of  $2.4/69.2 = 0.035\%$ . Selective harmonic elimination (SHE) modulation technique can be used to completely remove the existence of the remaining harmonics (5th, 11th and 13th) from the output voltage and current [25]. It must be addressed that the estimation and eradication of harmonics is not a purpose of this manuscript.

The experimental results obtained in Figure.10b that the RMS value of the fundamental frequency components has decreased by 22% at a slightly higher THD since, the modulation index is reduced to  $m = 0.8$ . Reducing the modulation index to  $m = 0.3$  in Figure.11 a, it can be observed that the hybrid inverter has produced 7-level output voltage.

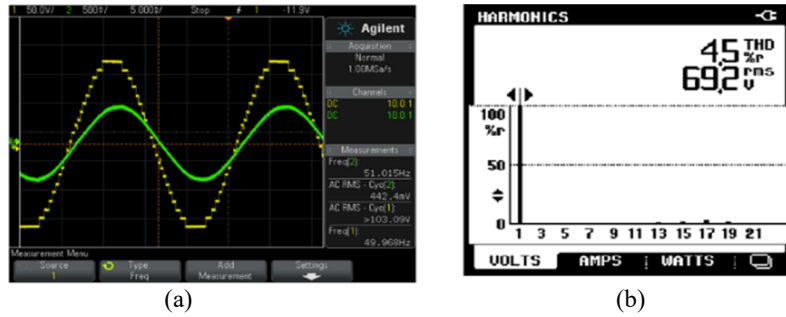


Figure 9. Experimental results at,  $m = 1$ : (a) output voltage and current and (b) harmonic spectrum.

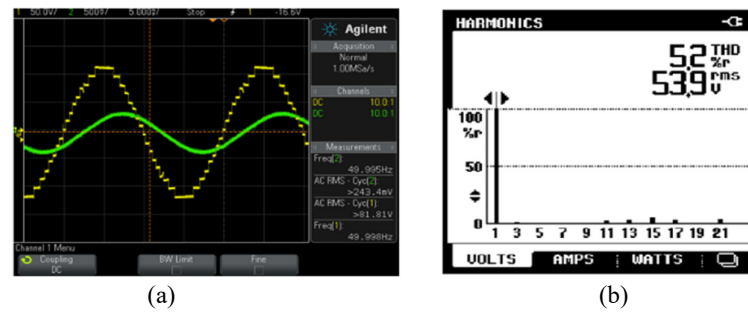


Figure 10. Experimental results at,  $m = 0.8$ : (a) output voltage and current and (b) harmonic spectrum.

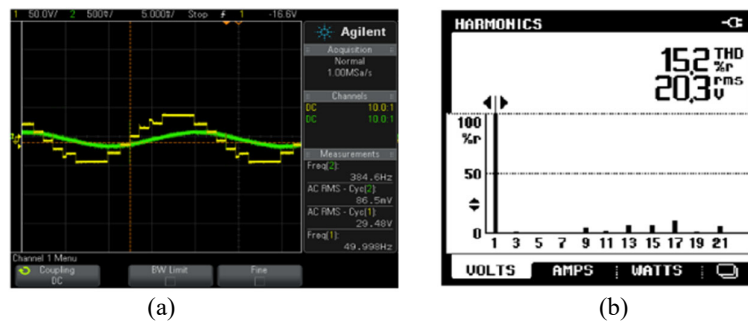


Figure 11. Experimental results at,  $m = 0.3$ : (a) output voltage and current and (b) harmonic spectrum.

In this case, the proposed inverter will operate exactly like the 7-level cross-switched inverter proposed in [13]. However, THD has increased significantly at  $m = 0.3$  while the RMS value of the fundamental frequency has decreased. Finally, a brief comparison between these results and the simulated results from the previous section is summarized in Table 5. By observing Table 5, it can be verified that in terms of output voltage, RMS voltage and THD, the highest deviation between the simulated results and the experimental results are relatively low. Therefore, it can be concluded that the obtained results from both simulation and hardware prototype is accurate and valid. The detailed experimental setup is shown in Figure 12.

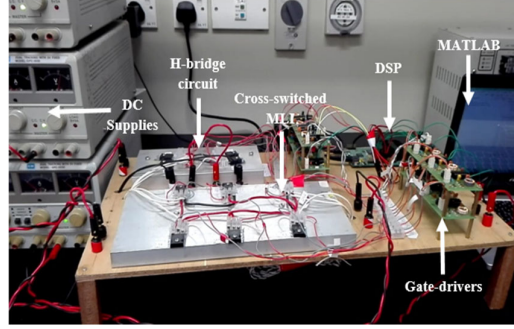


Figure 12. Experimental setup of the hardware prototype.

## 7. CALCULATION OF LOSSES

The newly developed hybrid inverter contains ten IGBTs each having one anti-parallel diode. Because of this, the hybrid topology generates two major forms of power losses which are conduction losses and switching losses. MLI's conduction losses arise when the IGBT devices are at on-state. The rapid conduction losses of the IGBTs and diodes are calculated using, (14) and, (15) respectively.

$$IGBT(t) = [V_{IGBT} + R_{IGBT} i(t)] \times i(t). \quad (14)$$

$$Diode(t) = [V_{Diode} + R_{Diode} i(t)] \times i(t). \quad (15)$$

Here,  $V_{IGBT}$  is the on-state voltage of IGBTs and  $V_{Diode}$  is the on-state voltage of the diodes.  $R_{IGBT}$  and  $R_{Diode}$  represents the corresponding resistance of the IGBTs and the diodes. The entire conduction losses ( $P_{conduction}$ ) of the hybrid MLI is determined by adding the  $IGBT(t)$  and  $Diode(t)$ .

The switching losses ( $P_{switch}$ ) of the MLI is determined by calculating the amount of power consumption from the IGBTs when they are turning on and off. This loss is only considered for the IGBT devices because diodes do not produce these losses. The energy loss symbolized by turn on ( $E_{on}$ ) and turn off ( $E_{off}$ ) of IGBTs are determined by using (16) and, (17).

$$E_{on} = \int_0^{t_{on}} \left[ \left( \frac{v_{switch}}{t_{on}} t \right) \left( -\frac{I}{t_{on}} (t - t_{on}) \right) \right] dt. \quad (16)$$

$$E_{off} = \int_0^{t_{off}} \left[ \left( \frac{v_{switch}}{t_{off}} t \right) \left( -\frac{I}{t_{off}} (t - t_{off}) \right) \right] dt. \quad (17)$$

Here, current of the turned on IGBT devices are designated by  $I$ .  $v_{switch}$  demonstrates the forward voltage drop of the IGBTs whereas,  $t_{on}$  and  $t_{off}$  symbolize the turn on and turn off period for the IGBTs. Therefore, the entire switching loss can be determined applying (18).

$$P_{switch} = f \left[ \sum_{i=1}^{N_{switch}} \left( \sum_{i=1}^{N_{on}} E_{on,i} + \sum_{i=1}^{N_{off}} E_{off,i} \right) \right] \quad (18)$$

Here,  $N_{on}$  and  $N_{off}$  symbolize the amount each IGBT is turning on and off through a time period of  $t$ . Therefore, the total loss ( $P_{hybrid}$ ) of the proposed inverter can be determined as follows;

$$P_{hybrid} = P_{conduction} + P_{switch} \quad (19)$$

In this papers, ABB5SNG class of switching devices are utilized. This model of IGBT has the following parameters;  $V_{IGBT} = 2.4\text{v}$ ,  $R_{IGBT} = 0.052 \Omega$ ,  $V_{diode} = 2 \text{ V}$  and  $R_{diode} = 0.1 \Omega$ . The overall power loss of the hybrid MLI is calculated by following a total output voltage of 100.3 V compromising a single phase resistive-inductive (R-L) load having  $100 \Omega$ -0.23 H as output. Therefore, the MLI is able to deliver 50.34 W output power (14 mW/sec). Using the configurations stated above and using (14) to (19) the total losses of the hybrid inverter is evaluated 0.34 mW/sec. Thus, the efficiency of the hybrid MLI is 97.52% operating for 1 second.

Table 5. Summary of output results

Modulation index ( $m$ )	Output voltage (V)		RMS voltage (V)		THD (%)	
	Simulation	Experimental	Simulation	Experimental	Simulation	Experimental
1.00	100.30	102.51	70.95	69.20	3.90	4.50
0.80	80.39	81.81	56.84	53.90	4.84	5.20
0.30	30.62	29.48	21.65	20.30	12.33	15.20
Maximum deviation	2.20%		5.45%		23.28%	

## 8. CONCLUSION

The establishment of a hybrid MLI compromising the capability to generate 21-step output voltage utilizing less amount of power devices is the primary impact of this manuscript. The effective utilization of the modified low frequency modulation technique and the extremely precise simulation and experiment results confirmed that this MLI's performance is extremely proficient and consistent. The enhancement of the performances and consistencies of the MLI topologies are becoming a foremost issue because the necessities and various applications of MLIs are radically growing every day. Being, one of the most appreciated machineries in the area of power electronics, the projected hybrid MLI can be applied as a foremost device in different industries. Finally, it must be mentioned that this hybrid MLI can be further improved to generate increased voltage steps and can be studied in the forthcoming researches.

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